

DRAFT

SG84

STE Advanced Colour Graphics

User's Manual

Contents

Section	Page
1. Introduction	3
2. Circuit Description	4
3. Links and Options	6
4. I/O Map	9
5. Using the SG84	10
6. Fault Finding Guide	17
Appendix	
A. Component List	19
B. Connections	20
C. Specification	23
D. Circuit Diagram	

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Revision History

Manual	PCB	Comments
v1 iss 2	v1 iss 2	Design MJS Layout AJL Manual KH 880314 First laser typeset in this format

Section 1. Introduction

The SG84 is a fast, high resolution colour graphics board. It contains an advanced display controller and powerful graphics optimised processor in a single chip, the Hitachi 63484 ACRTC.

The graphics processor uses hardware and microcode to perform very high speed pixel operations, including lines, arcs, ellipses, filling, and block transfers.

The display controller provides an upper, lower and middle base screen, one window, and zooming, directly from hardware. The cursor can be a block-cursor, up to two cross-hairs, as chosen by software.

The resolution is programmable (up to 640x256 non-interlaced, 640x500 interlaced) in either 16 or 256 logical colours, from a palette of over a quarter of a million (262144 to be exact) physical colours. This allows a range of special effects such as instant colour changing, or 'false colour' images. Colours can also be made to flash.

The SG84 supports two frame-access modes. In single-access mode the user can choose between flicker-free display-priority mode where drawing is stopped during display periods, or the faster drawing-priority mode where drawing may occur during display periods. In dual-access mode, display and drawing accesses are interleaved, allowing fast drawing at any time without disturbing the display. This is only available to 16-colour displays.

The 256k of on-board memory provides either one 256-colour screen, or two 16-colour screens. Any memory not used for display can be used to hold fonts, icons, windows etc.

The SG84 provides analogue and TTL level video signals (RGB or monochrome) with selectable sync polarity.

This manual provides a description of the SG84 board, an ACRTC command summary, and some example programs. For a more detailed description of the ACRTC registers and commands, see the document titled "HD63484 ACRTC Advanced CRT Controller User's Manual" available from Hitachi or distributors of the ACRTC.

Video Shift Registers

The pixel shift registers are four PALs, IC29-30, which load eight bits each at a time and shift these out at a rate determined by the pixel shift clock. These PALs have two extra pins to select 4 or 8-bit pixels (16 or 256-colour mode), and to disable pixel shifting (when horizontal zooming by a factor of n , all but every n th pixel shift is disabled). Two other input bits affect the output stream - the flashing bit inverts the data stream, and the cursor bit makes the outputs tristate, producing a pixel value of &FF.

High Speed Video Colour Palette

This chip contains a colour look-up table (256 words of fast RAM) driving three high speed DACs to produce the red, green and blue analogue outputs for the video display. The user may have 16 or 256 different logical colours on the screen simultaneously, each of which may be any one of 262144 physical colours. The outputs produce a 1.0V video signal when driving a 75 Ω load. Composite syncs can be superimposed on the analogue red, green and blue signals (RGB) by making LK12.

The SG84 also provides TTL level RGB video signals. These are taken directly from the shift register outputs, so no palette techniques can be used with TTL outputs. IC25 controls the inversion of colour signals, the inversion, mixing and superimposition of syncs, and blanking.

Frame data store, eight 64k x 4 bit DRAMs, IC12-15 and IC20-23

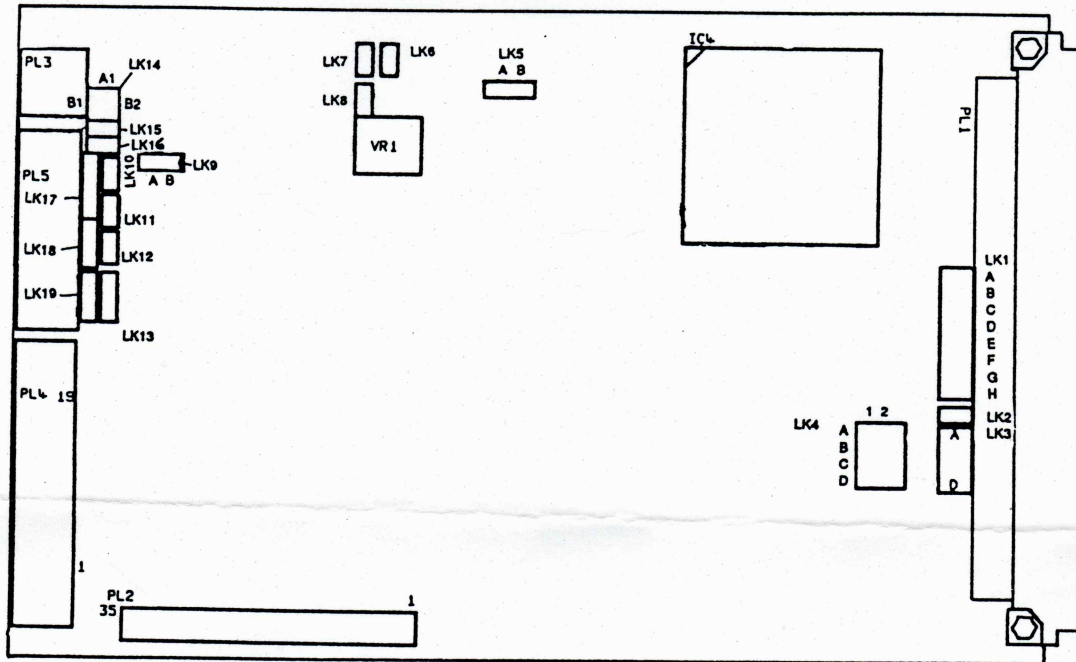
$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ strobe in the multiplexed address lines from the ACRTC. $\overline{\text{OE}}$ is held inactive to prevent the DRAM outputting data while $\overline{\text{WE}}$ is asserted to write data in after $\overline{\text{CAS}}$ has been asserted. 4-bit wide DRAMs reduce the minimum number of chips needed for a working design. The DRAMs are arranged in a 16-bit wide bus to the ACRTC and in a 32-bit wide bus when performing display cycles - this requires that the GAI (graphics address increment mode) be set to 2. Apart from this, the bus width difference is transparent to user software.

Section 3. Links and Options

The boards are described as if you were viewing them from the component side with PL4 to the right.

Note: + indicates the standard link connection, as supplied.
 * indicates a signal is active low

Link positions



Link area 1. Base Address selection

- LK1H select if A4 low
- + LK1G select if A5 low
- + LK1F select if A6 low
- LK1E select if A7 low
- LK1D select if A8 low
- LK1C select if A9 low
- + LK1B select if A10 low
- + LK1A select if A11 low

Standard jumpering as shown above gives a base address of 390 (hex) or 912 (decimal). Note that some operating systems may not access this board at the standard address. You **MUST** check with the appropriate software manual.

Link area 1.

o	A	o
o	B	o
o	C	o
o	D	o
o	E	o
o	F	o
o	G	o
o	H	o

LK1 sets up the standard base address of the SG84 in STE I/O space. The standard base address is 390 (hex). If a jumper on link 1 Inserting a jumper on link 1 means the board will only respond if that address line is low, omitting a jumper means the board will only respond if that address line is high.

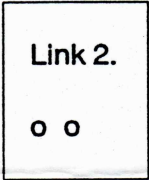
Table 1. Address Weights

LK1	Address Line	Hex	Dec
H	A4	10	16
G	A5	20	32
F	A6	40	64
E	A7	80	128
D	A8	100	256
C	A9	200	512
B	A10	400	1024
A	A11	800	2048

Link 2. DATAK* to STEbus

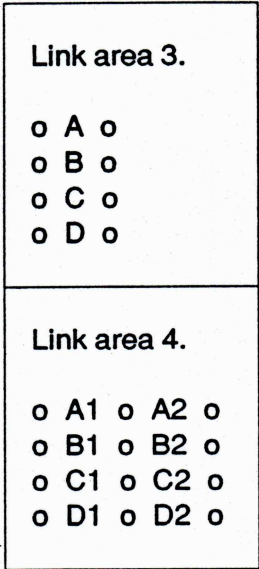
+ LK2 DATAK* goes to STEbus

Remove this link only when the expansion connector is being used.



Link areas 3 and 4. Interrupt and DMA Attention request outputs

- LK3A Interrupt request output on ATNRQ0*
- LK3B Interrupt request output on ATNRQ1*
- LK3C Interrupt request output on ATNRQ2*
- LK3D Interrupt request output on ATNRQ3*
- LK4A2 Interrupt request output on ATNRQ4*
- LK4B2 Interrupt request output on ATNRQ5*
- LK4C2 Interrupt request output on ATNRQ6*
- LK4D2 Interrupt request output on ATNRQ7*
- LK4A1 DMA transfer request output on ATNRQ4*
- LK4B1 DMA transfer request output on ATNRQ5*
- LK4C1 DMA transfer request output on ATNRQ6*
- LK4D1 DMA transfer request output on ATNRQ7*



Section 4. I/O Map

The STEbus has a total of 4096 possible I/O addresses, corresponding to a 12-bit address bus. There are six I/O addresses to which the board will respond. The upper 8 bits of the 12-bit I/O address are set by jumpers, as described in the previous section, and the remaining four bits of the I/O address define the group of I/O addresses to which the board responds. The table below shows the I/O addresses and the meaning of the bits at each address.

Table 1. I/O Addresses

Address	Rd/Wr	bit	Function
base	Wr	0-7	ACRTC Address register
	Rd		ACRTC Status register
		0	Write-FIFO Empty
		1	Write-FIFO Ready
		2	Read-FIFO Ready
		3	Read-FIFO Full
		4	Light Pen Strobe Detect
		5	Command End
		6	Area Detect
		7	Command Error
base+1	Rd/Wr	0-7	ACRTC Data register
base+2	Rd/Wr	0-7	Accesses to this location perform a DMA cycle with the ACRTC
base+3	Rd/Wr	0-7	Repeat of above. Non-preferred address
			Palette:
base+4	Wr	0-7	Address register. Write the 8-bit logical colour number to this location.
base+5	Wr	0-7	Colour Value register Write the red, green, blue values to this location (in that order), then these will be loaded into the colour look-up table and the address register (above) automatically incremented.
base+6	Wr	0-7	Mask register Incoming pixels from the shift registers are logically ANDed with the mask register before being sent to the colour look-up table.

Section 5. Using the SG84

To use the SG84 the ACRTC control registers must first be initialised, the palette must be programmed and finally drawing commands must be issued to produce screen output.

5.1. ACRTC Registers

There are three main groups of registers:

5.1.1. Hardware accessible registers.

These are accessed at STEbus I/O locations, as described in Section 5. I/O Map.

5.1.2. Direct address registers.

All these registers are accessed by first writing the register number to the ACRTC address register, then the required value to the data register. They can be sub-divided as follows:

a: General control registers: r00H - r06H

r00H - the FIFO entry register enables access to FIFO accessible, (command accessible) registers.

r02H - the command control register controls overall ACRTC operation such as aborting, defining DMA protocols and enabling/disabling interrupt sources.

r04H - the operation mode register defines basic parameters of ACRTC operation such as frame buffer access mode, display or drawing priority etc.

r06H - the display control register independently enables or disables each of four logical display screens and also contains 8 bits of extra video attributes specific to the SG84.

b: Timing control registers: r80H - r9CH

These registers define ACRTC timing, including specification for CRT control signals, logical display screen size and display period.

c: Display control registers: rC0H - rEEH

These registers define logical screen display parameters such as start addresses and memory width. Also included are the cursor definitions, zoom factors and light pen registers.

Writing to registers 80H onwards will automatically increment the value of the address register by one. 16 bit registers and data are transmitted as two groups of 8 bits, high byte first, low byte second.

5.1.3. FIFO accessible (command accessible) registers (16 bit)

All these registers are accessed via the read and write FIFOs, using the ACRTC commands read pattern RAM, write pattern RAM, read parameter register and write parameter register.

a: Pattern RAM: 00H - 0FH

Pattern RAM is used to define drawing and painting 'patterns'. 16 x 16 bits of data may be sent to the pattern RAM, and all drawing operations will then interpret this information according to the values stored in the pattern RAM control registers and the colour registers where 0 (bit not set) corresponds to CL0 and 1 (bit set) corresponds to CL1. Thus, setting both colour registers to the same value will produce solid, one-colour drawing irrespective of the information in the pattern RAM.

b: Drawing parameter registers: pr00H - 13H

These registers define detailed parameters of the drawing process, such as colour control, area control and pattern RAM pointers.

5.2. Initialisation

5.2.1. General Control Registers

To initialise the ACRTC, the general control registers must first be set up for the operation and access modes required. Some of these require specific explanation.

Graphic bit mode (CCR, high-order, bits 6-4):

4 bits per pixel means that for each of the 640 pixels displayed across the screen, 4 bits of frame buffer information are required. Each of these logical pixels can therefore hold the value 00H to 0FH, corresponding to the 16 definable colours in the palette look-up table.

In 8 bit mode each pixel requires 8 bits of frame buffer information. These can hold the value 00H to FFH, corresponding to the 256 colours in the palette look-up table.

This means that in 4 bits per pixel mode half as much RAM is required to display the same number of pixels as in 8 bits per pixel mode.

For example, if the whole screen is cleared to colour 1, one 16-bit word read from that area would hold the value:

1111H - 4 bit mode (4 pixels)
0101H - 8 bit mode (2 pixels)

Access mode (OMR, low order, bits 3-2):

In 4 bits per pixel mode you should interleave the drawing and display functions (dual access mode 0). In 8 bit mode single access needs to be selected (with display priority) otherwise picture interference would occur while drawing.

Attribute control (DCR, low order, bits 7-0):

Some of these bits are hardware specific to the SG84:

Bit 0 defines the cursor type: 0 = crosshair, 1 = block cursor
(cursor type also needs to be defined in CDR, rE8H)

Bit 1 defines the graphic bit mode: 0 = 4 bit mode, 1 = 8 bit mode
(this needs to be set to the same mode as defined in the CCR)

Bit 2 provides TTL output to pin 1 of PL5

5.2.2. Timing Control Registers

The timing control registers must be initialised to display at least the base screen, although they are also used to initialise the upper and lower screens, and the window if required. Positioning of these screens can only be done on 32-bit word boundaries relative to the base screen.

Horizontal timing calculations:

	SET VIA
LINE PERIOD = 64 us = 100%	HC (Horizontal cycle)
HSYNC = 5.12 us = 8%	HSW (Horizontal sync width)
BACK PORCH = 5.12 us = 8%	HDS (Horizontal display start)
ACTIVE DISPLAY PERIOD = 51.2 us = 80%	HDW (Horizontal display width)
FRONT PORCH = 2.56 us = 4%	REMAINING TIME

Frame buffer cycle time is 320 ns for a 25MHz crystal:

$$\frac{4 \text{ pixels/word}}{12.5 \text{ MHz/pixel}} = 320 \text{ ns/word}$$

1) Line period

$$64 \text{ us required: } 64\text{us}/320\text{ns} = 200 \text{ cycles}$$

$$\text{HC} = 200 - 1 = \text{C7H}$$

2) Horizontal sync period

$$5.12 \text{ us required: } 5.12\text{us}/320\text{ns} = 16 \text{ cycles}$$

$$\text{HSW} = 10\text{H}$$

3) Back porch

$$5.12 \text{ us required: } 5.12\text{us}/320\text{ns} = 16 \text{ cycles}$$

$$\text{HDS} = 16 - 1 = 0\text{FH}$$

4) Active display period

$$51.2 \text{ us required: } 51.2\text{us}/320\text{ns} = 160 \text{ cycles}$$

$$\text{HDW} = 160 - 1 = 09\text{FH}$$

5) Front porch

$$= \text{HC} + 1 - (\text{HSW} + \text{HDS} + 1 + \text{HDW} + 1) = 10 \text{ cycles at } 210 \text{ ns}$$

$$= 3.2 \text{ us}$$

Thus, the values sent to the horizontal timing registers are:

Horizontal Sync register (r82H): C710H

Horizontal Display register (r84H): 0F9FH

Vertical timing calculations:

Typically the vertical flyback period occupies about 7% of the vertical period. In the case of the 312 line system example (ie 625 lines, non-interlaced), 20 lines are lost per frame. As the resolution is to be 256 lines, the front and back porches will be 18 lines each.

- 1) Frame rasters
312 lines required
VC = 138H
- 2) Front porch
18 lines required
VDS = 18 - 1 = 11H
- 3) Vertical sync period
20 lines required per display field
VSW = 14H
- 4) Display period
256 lines required
SP1 = 100H
- 5) Back porch
= VC - (VDS+1 + SP1 + VSW) = 18 lines

Thus, the values sent to the vertical timing registers are:

Vertical Sync register (r86H): 0138H

Vertical Display register (r88H): 1114H

Split Screen Width Register (r8AH): 0100H

5.2.3. Display Control Registers

The display control registers must be initialised for at least the base screen. This involves setting up the start address register (SAR1, high and low bytes) with the physical memory address which will correspond to the top left pixel on the screen, and the memory width register (MWR1) with the number of 16-bit words to display 1 line of pixels. The memory width is thus dependant on the number of bits per pixel - ie divide the number of horizontal pixels required by 4 for 4 bits per pixel, or 2 for 8 bits per pixel.

The SG84 has 256K of frame buffer memory available. In 4 bits per pixel mode, with 640 pixels horizontally (ie 320 bytes) and 256 pixels vertically, the screen display requires about 82K, leaving 174K extra, which means that drawing is possible outside the displayed area. It is possible to display this extra memory by altering the start address, to produce a scrolling effect. _

If the memory width is defined as equal to the display width, only vertical scrolling is possible. If it is defined as greater than the display width, horizontal scrolling is also possible.

After this initialisation procedure, before any drawing is attempted, it is necessary to clear the display area and define a logical origin. These operations require the use of ACRTC commands which are described below.

5.3. Setting up the palette

A palette is simply a colour look-up table. The pixel data from the DRAM is bitwise ANDed with the pixel mask register to form an 8-bit address to a high speed RAM. The 18-bit data from this RAM (6 bits each for red, green and blue respectively) is sent to three 6-bit high-speed D to A converters, which provide the analogue voltage to drive the three colour guns of the monitor. By changing the data in the palette, you can redefine the physical colours produced by the logical pixels.

The palette can be programmed with 16 (4 bits per pixel) or 256 (8 bits per pixel) groups of three intensity values, where 0 is no intensity for that colour, and 63 is maximum intensity.

The colour number register is used to specify the position in the look-up table to be written with a colour value. The colour value register contains the data used to update the contents of the colour number specified by the colour number register.

To write a new value to the table a colour number must be specified and then 18 bits of data written to that colour number in the table. This is done by writing a colour number to the colour number register, and then three successive byte writes to the colour value register. The least significant 6 bits are taken from each byte, the first defines the red intensity, the second the green and the last the blue. If the colour number register is modified during a colour value write sequence, the colour value register is initialised, aborting any unfinished write sequence.

The colour number register increments automatically after every colour value write sequence.

The colour number used to access the colour look-up table is the result of bitwise ANDing the incoming colour number and the contents of the pixel mask register. For example, if the incoming colour number is 3EH and the mask register contains 0FH, the resulting colour number selected will be 0EH. Thus the displayed colours can be altered without altering the look up table, to produce, for example, flashing objects.

5.3.1 'False colours'

There are a variety of uses for a palette. One can for instance take a grey-level image and assign a 'false' colour to each level in order to highlight details or contours. This would be useful in thermography, with colours representing temperature levels (say blue = cold, red = warm).

5.3.2 'Invisible Ink' drawing

Another palette trick is the use of 'invisible ink' drawing. The pixel mask register can be set to &7F, so that colours 128-255 appear the same as colours 0-127. An invisible image can be drawn by setting bit 7 of affected pixels. When this image has been completely drawn, colours 128-255 can be redefined (e.g. as red). When the pixel mask register is set to &FF, all the affected pixels will appear on the screen simultaneously. This trick is useful in real-time animations, because the image is not seen until it has been completely drawn. It also

gives the illusion that the computer is much faster than it actually is, as it appears to the viewer that the image is being redrawn instantly, whereas in actual fact it may use up to all the time between successive frames to generate each frame.

5.3.3 'Translucent' colours

Similar to the example above, but the top half of the palette is a reduced intensity copy of the bottom half, tinted with a desired colour. Hence logical pixels with bit 7 set appear to be translucent to a background image.

5.4. Drawing commands

ACRTC commands consist of a 16-bit operation code, optionally followed by one or more 16-bit parameters. Commands, parameters and data are sent to and from the ACRTC high byte first, low byte second. The low 8 bits of the operation code may be used to define area, colour and operation modes, where area defines the logical x,y coordinates within which drawing will appear on the display, colour determines the way in which the colour registers are interpreted and operation determines whether the drawing will be done in AND, OR, XOR mode etc. ACRTC drawing commands can be classified into three groups:

5.4.1. Register access commands

Registers associated with drawing (pattern RAM and drawing parameter registers) are accessed using the register access commands. These are the origin command, read and write parameter register, and read and write pattern RAM.

5.4.2. Data transfer commands

Data transfer commands are used to move 16-bit word data between memory and the frame buffer, or within the frame buffer itself. The horizontal coordinates of these commands relate to word values across the screen, so they are dependant on the graphic bit mode. Before issuing these commands, a physical 20 bit frame buffer address must be specified by the RWP (read/write pointer) in the drawing parameter registers. They include commands to clear, copy and modify words of data in the frame buffer, and to read and write words directly.

5.4.3. Graphic drawing commands

Graphic drawing is performed by modifying the contents of the frame buffer based upon microcoded drawing algorithms in the drawing processor. There are 23 graphic drawing commands, including commands to move, draw a line, draw a circle etc. They use logical x,y coordinates relative to the most recently defined origin.

Further discussion of the properties of the ACRTC are beyond the scope of this document. For further information refer to the Hitachi HD63484 ACRTC Advanced CRT Controller User's Manual.

5.5. Monitors

The SG84 is designed to be used with a monitor with analogue colour inputs, in order to take full advantage of the palette colour range. The SG84 can also drive a standard TTL-compatible RGB monitor. These are inherently limited to 8 colours, plus intensity. In this case connect the monitor signals (R,G,B,COMPSYNC,GND) to PL4 (as shown in Appendix B. Connections). These outputs are driven by the logical pixel value, since the physical pixel value is internal to the palette chip, so no palette techniques can be used with this type of monitor.

The SG84 may be used with the following monitors:

- a: Analogue RGB - from PL4
- b: TTL RGB and intensity (palette bypassed).
Available on PL5, and linkable to PL4 in place of analogue.
- c: Composite video, gray scale (palette bypassed) generated from TTL RGB outputs.
Available on PL3.

International Video Standards

In countries using a different video standard to the U.K., it is usually possible to modify the board to work with these standards by simply re-programming the ACRTC registers. For example, in the U.S.A. the line period is the same, but the frame period is shorter. In countries where the line period is considerably different to the U.K., it will probably still be possible to sync. with a monitor, but the picture may be the wrong size.

Section 6. Fault Finding Guide

All Arcom boards are thoroughly inspected and soak-tested before despatch, and so the likelihood of a board being faulty on arrival is small.

If the board has never worked, it is possible that it was damaged in transit, so please inspect it carefully for physical damage before proceeding with this guide.

Fault	Cause	Remedy
No picture.	No power. Faulty connector(s).	Check power to SG84 and monitor Check that the RGB signals are reaching the monitor.
Blank screen	Wrong initialisation.	Are you sure that you have sent the right bytes ?
Accesses to the board 'hang'.	Wrong address. Faulty bus or socket.	Check that the address being used corresponds to the jumpers in LK1
Picture too large	Incorrect clock frequency or maladjusted monitor	Adjust clock frequency or monitor.
Jumping picture	Wrong video standard.	Is your monitor compatible with the video standard ?
Wavy picture	Bad syncs.	Check that you are supplying your monitor with all the syncs it needs, and that they are of the correct polarity. Check that they are reaching the monitor.
Skewed picture	External EMI	Check that the monitor that you are using is set up to work with standard U.K. line and frame rates. Is the SG84 close to any sources of strong electro-magnetic interference (for example the monitor or a switched-mode power supply)? Try moving any possible sources away or shielding the board better.

Fault	Cause	Remedy
Skewed picture.	Bad ground.	A bad picture is usually the result of an insufficient ground between the output device and the monitor. Check that you have connected the ground from SG84 PL4 pin 8 to your monitor input ground (this is not necessarily the same ground as the monitor's case).
Frequency mismatch.		Check that your monitor is working at the correct frequency.

Appendix B. Connections

PL1. STEbus 64-way a/c DIN41612

(for suitable backplanes refer to current catalogue).

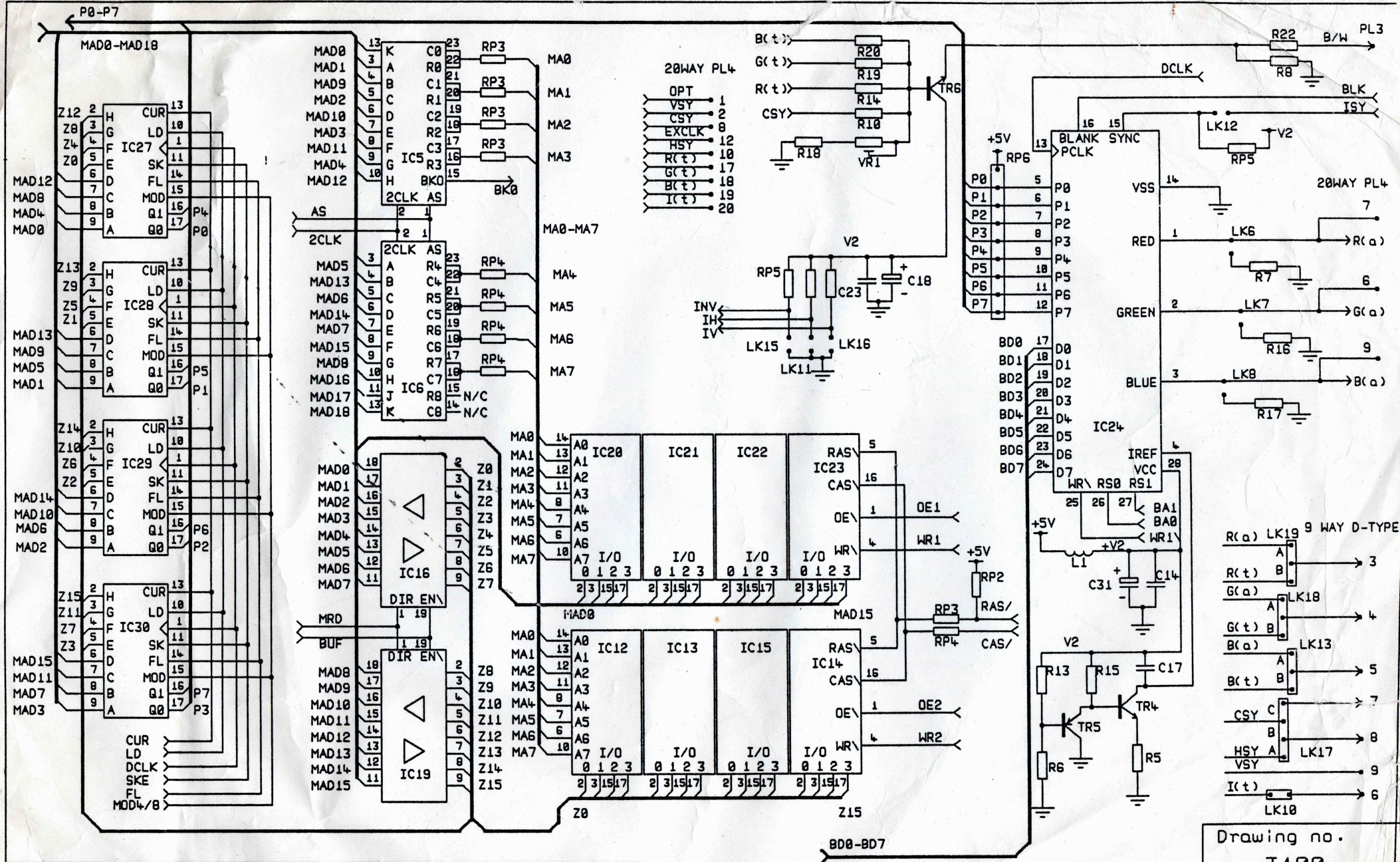
Pin		Row a c	
1	GND	o o	GND
2	+5V	o o	+5V
3	D0	o o	D1
4	D2	o o	D3
5	D4	o o	D5
6	D6	o o	D7
7	A0	o o	GND
8	A2	o o	A1
9	A4	o o	A3
10	A6	o o	A5
11	A8	o o	A7
12	A10	o o	A9
13	A12	o o	A11
14	A14	o o	A13
15	A16	o o	A15
16	A18	o o	A17
17	CM0	o o	A19
18	CM2	o o	CM1
19	ADRSTB*	o o	GND
20	DATAACK*	o o	DATSTB*
21	TRFERR*	o o	GND
22	ATNRQ0*	o o	SYSRST*
23	ATNRQ2*	o o	ATNRQ1*
24	ATNRQ4*	o o	ATNRQ3*
25	ATNRQ6*	o o	ATNRQ5*
26	GND	o o	ATNRQ7*
27	BUSRQ0*	o o	BUSRQ1*
28	BUSAK0*	o o	BUSAK1*
29	SYSCLK	o o	VSTBY
30	-12V	o o	+12V
31	+5V	o o	+5V
32	GND	o o	GND

PL5. 20-way video output edge connector

OPT	1	o o	2	VSYNC
DISP1	3	o o	4	DISP2
EXSYNC	5	o o	6	G(ana)
R(ana)	7	o o	8	CSYNC
B(ana)	9	o o	10	HSYNC
Gnd	11	o o	12	EXCLK
Gnd	13	o o	14	LPSTB
+5	15	o o	16	+5
R(TTL)	17	o o	18	G(TTL)
B(TTL)	19	o o	20	I(TTL)

Appendix C. Specification

Operating temperature	5 C to 55 C (non-condensing)
Power consumption (typ)	5V +/- 0.25V 2.8 A
Video output	RGB (TTL), analog, monochrome
Colours	16 or 256 programmable
Palette	256 of 262144 physical colours
Memory	256 kbytes
Access mode	single (256-colour mode) dual (16-colour mode)
Zooming	Up to x16 horizontal and vertical
Bus	STEBus
Bus connector	64a/c DIN 41612
Format	Single Eurocard
Dimensions	183mm x 100mm x 14mm
Weight	208g



Date Drawn	880104	Date Checked		Date Approved	880106	Date This copy for	
Version	1	1					
Issue	1	2					
Date	880104	880307					

Title SG84

SHEET 2 OF 2

Drawing no.
J100

Arcom
CONTROL SYSTEMS LTD.

1 R
2 G
3 B
4 CSYNC
5 GND